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United States Patent [19][11] **Patent Number:** **5,834,848****Iwasaki**[45] **Date of Patent:** **Nov. 10, 1998****[54] ELECTRONIC DEVICE AND SEMICONDUCTOR PACKAGE**[75] **Inventor:** Ken Iwasaki, Yokohama, Japan[73] **Assignee:** Kabushiki Kaisha Toshiba,
Kanagawa-ken, Japan[21] **Appl. No.:** 982,417[22] **Filed:** Dec. 2, 1997**[30] Foreign Application Priority Data**

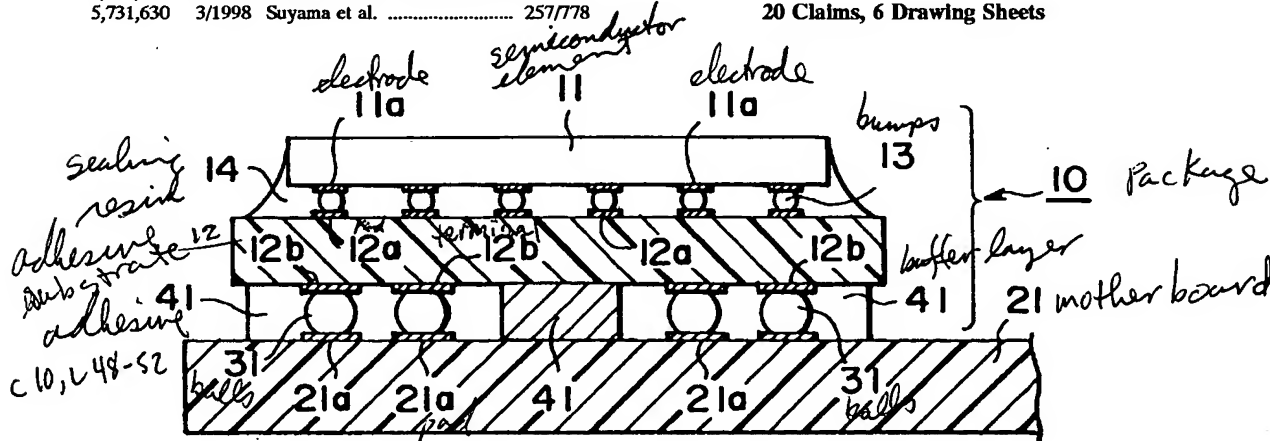
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[51] **Int. Cl.⁶** H01L 23/48; H01L 23/52;
H01L 29/40[52] **U.S. Cl.** 257/778; 257/780[58] **Field of Search** 257/781, 777, 779, 686, 782, 697**[56] References Cited****U.S. PATENT DOCUMENTS**

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Primary Examiner—Mahshid D. Saadat*Assistant Examiner*—S. V. Clark*Attorney, Agent, or Firm*—Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P.**[57] ABSTRACT**

The electronic device has a structure that a semiconductor package (10) is mounted on a motherboard (21), and a buffer layer (41) for relieving a stress, which is produced due to a difference of physical properties between the semiconductor package (10) and the motherboard (21), is mounted on the electrical and mechanical interface between the semiconductor package (10) and the motherboard (21). For example, the buffer layer (41) having a thermal expansion coefficient close to that of the motherboard (21) is formed on a face of the semiconductor package 10 having an external connecting terminals (12b) mounted. A stress caused due to a difference between a thermal expansion coefficient of a wiring substrate (12) of the semiconductor package and that of the motherboard (21) can be relieved by the buffer layer (41). Therefore, a cyclic stress applied to the connection between the semiconductor package and the motherboard in the actual application environment can be relieved, and reliability of connection can be improved. Thus, a semiconductor package mountable with a high degree of reliability and an electronic device having a high degree of reliability is provided.

20 Claims, 6 Drawing SheetsFig. 9